

ECMA-253 Interface Converter/ Octet Timing Regenerator

This equipment together with a PT50x Protocol Tester, is currently used by ANSPs and VCS Suppliers to perform ATS-QSIG conformance and interoperability testing. Its Octet Timing re-generation option however guarantees octet integrity for those ANSPs leasing 64kbit/s data circuits or employing the IP network for transport of their octet information.

Functionality

The G.703-EIA530 converter module automatically synchronizes and maintains synchronization to a G.703 64kbit/s co-directional line either through :

- Ø a received 8KHz octet timing signal (with code violations indicating octet delimiters in order that the position of 8-bit octets within the serial bits stream can be determined) or
- Ø a built-in HDLC flag search algorithm able to identify the position of the received 2 bit D_Q signalling channel through an HDLC flag search within the full 64kbit/s bit stream, which then enables the position of 8-bit octets to be located;

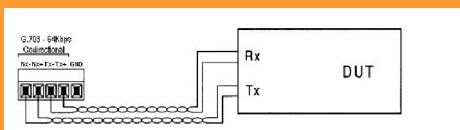
As an optional added functionality the G.703-EIA530 converter module is also able to re-generate an 8KHz octet timing signal with appropriate Octet violations when receiving bit-serial data from a circuit that can't guarantee octet integrity.

The module is also able to recovery from both an odd or even number of bit slips in the 64kbps bit stream

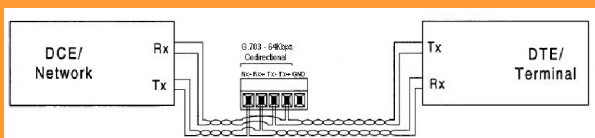
An ECMA 253 interface converter has a front panel rotary switch that allows selection of the following 3 distinct modes:

Operating modes

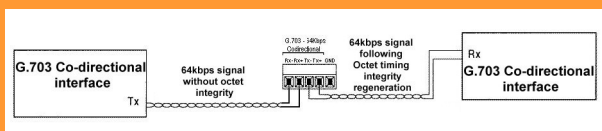
Emulation Mode: Synchronizes a PT50x protocol tester to a 64kbps digital unrestricted co-directional line (D64U) connected to an ATS-QSIG interface card within a VCS in order to perform conformance testing or protocol emulation tests.



Monitor Mode: Employs high impedance to synchronize a PT50x protocol tester to a 64kbps digital unrestricted co-directional line (D64U) linking two ATS-QSIG interface cards in order to perform interoperability testing.



Octet Timing Regeneration Mode (Option): Allows re-generation of an 8KHz octet timing signal from an incoming 64kbps digital unrestricted co-directional line without octet violations, but containing HDLC flags in its ECMA-253 compliant 16kbps D_Q signalling channel.



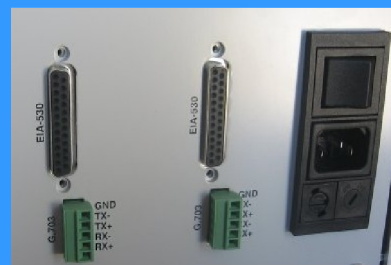
Physical description

The standard ECMA-253 converter rack is 6 slot 3U rack mountable system fitted with a power supply module and two G.703 EIA530 converter modules. 3 expansion slots allows expansion with further G.703-EIA530 converter modules or the LD-CELP voice monitoring module.

A table top standalone version of a G.703-EIA530 converter module is also available powered by an AC/DC mains adapter

Five front panel LEDs indicate the Power ON state, Rx line activity, Tx line activity, Octet Timing Sync and/or HDLC sync.

A removable 5 screw terminal block on the rear panel permits easy connection of G.703 64kbit/s co-directional Tx/Rx pairs while a EIA-530/DB25F socket supplies/receives the 16kbit/s D_Q signalling channel to/from the PT50x protocol tester.



The G.703-EIA530 module is a 6 layer printed circuit board with surface mount technology and a FPGA (Field programmable gate array) semiconductor device containing programmable logic. Through an on-board port it is possible for the supplier to re-program the FPGA with future enhanced functionality and updates. The module interfaces directly with the LD-CELP 3-channel voice monitoring module (option) within the rack.

Electrical Characteristics of the G.703 codirectional interface

- (**Interface:** ITU-T G.703 co-directional interface.
- (**G.703 Signal In and Out:** 2 wire symmetrical, electrically isolated, short-circuit protected, overvoltage protected
- (**Maximum Range:** Up to 800m over 24 gauge (0.5mm)
- (**Data Rate:** 64,000 bps (on G.703 co-directional line)
- (**Line Signal Coding:** 64kbps Codirectional line code
- (**Control Signals:** None
- (**Impedance:** 120Ω balanced (G.703 Emulation Mode), 1.2KΩ balanced (G.703 Monitor Mode).
- (**Clock Frequency:** 64KHz +/-100ppm
- (**"Pulse" Amplitude:** 1.0V nominal +/- 10%
- (**"Zero" Amplitude:** 0V +/-0.1 V maximum
- (**Protocol:** Synchronous 16KHz (64KHz gated clock), full duplex and bi-directional monitor



Electrical Characteristics of the EIA-530 interface

- (**Interface type:** EIA-530 interface for connection to the Protocol Tester (using either DB25 to MB34 or DB25 to DB37 adapter cable supplied).
- (**Connector:** DB25/Female
- (**Data Rate:** 16,000 bps (containing only extracted D₀ signalling data)
- (**Data Type:** Balanced for V.35 and V.36 (RS.449)
- (**Impedance:** 120 Ω balanced (EIA-530)



Connectors

- (**G.703-EIA530 converter module:** One removable 5-screw terminal block with terminals for Transmit and Receive Pairs of codirectional interface and ground terminal;
- (**One DB25/Female connector:** to connect to PT50x protocol tester
- (**Power Supply module connectors:** One AC mains power inlet socket for connection of mains power lead (supplied)

Front panel Indicators

- (**G.703-EIA 530 module indicators:** 5 front panel LEDs: Power, Rx Signal, Tx Signal, OCT (synchronization with octet violations), HDLC (synchronization with HDLC flag search method).
- (**Rack Power Supply Module:** Power on/off LED (located within front panel button)

Front panel Switches

- (**G.703-EIA 530 module rotary switch:** 1 front panel rotary switch (used to select Emulation, Monitor, Octet Timing Regeneration (option) and OFF modes)
- (**Rack Power Supply module:** 1 front panel Power on/off button containing orange LED.

Rear panel Switches

- (**Rack Mains power switch:** 1 rear panel PWR on/off switch located above mains power inlet.
- (**Mains power selector:** 1 rear panel 120VAC-230VAC mains selector located below mains power inlet

Cables supplied

- (Either DB25 to MB34 or DB25 to DB37 adapter cable supplied)
- (Mains power cable



Synchronization delay parameters

- (**Delay for line synchronisation using Octet violation method:** 250 μs
- (**Delay for line synchronisation using HDLC flag search method:** 1 ms (detection of 2 consecutive flags)
- (**Loss of line synchronization using HDLC flag search method:** when no flag occurs in 200ms period
- (**Delay to synchronize to HDLC flags on non-detection of octet violations:** 1 ms (detection of 2 consecutive flags)
- (**Delay to synchronize using Octet violations when already synchronized using HDLC flag search:** 250μs (on detection of two consecutive octet violations)

Layer 2 HDLC flags

- (The layer 2 HDLC flag detection and decoding by G.703-EIA530 converter module compliant with EN 300 402-2 (ISDN; Digital Subscriber Signalling Systems No. One (DSS1) protocol; Data Link Layer; Part 2: General Protocol Specification- equivalent to ITU-T Recommendation Q.921 (1993), modified (1995));

Environmental characteristics

- (**Operating ambient temperature:** 0 to 50 deg. C
- (**Storage ambient temperature:** -20 deg. C to +75 deg C
- (**Operating Relative Humidity Tolerance:** 10 to 90%, non-condensing
- (**Storage Relative Humidity Tolerance:** 10 to 90%, non-condensing

Power Supply characteristics

- (**Rack Power Supply Module:** 120V - 230 VAC +/-15%, 45-55Hz, 1A
- (**120VAC or 240VAC mains:** rotary switch selector (positioned below mains inlet)
- (**Mains power supply fuse:** 1.5A rating (capsule positioned below mains inlet)
- (**Rack Power Supply Module fuse:** 1.25A rating (positioned within Power Supply Module)
- (**External AC/DC Power adapter:** 230 VAC +/-15%, 45-55Hz to 9VDC/500mA (supplied only with table top G.703-EIA 530 module unit)
- (**Rear panel earth terminal:** to connect rack to earth.

Dimensions and weight

- (**Rack Size:** 22.3 W x 17.8 D x 13.5 H (cm)
- (**Rack Weight:** 2 Kg (containing Power Supply module, Two G.703-EIA 530 modules);
- (**Table top G.703-EIA 530 module unit size:** 17,5 W x 13 D x 3 H (cm)
- (**Table top G.703-EIA 530 module unit weight:** 0.3 Kg (containing single G.703-EIA 530 module)
- (**Table top G.703-EIA 530 module circuit board:** 17 W x 10 D x 0.2 H (cm)



Tel/Fax:
+39 0736 39 90 56

Email:
info@jsp-teleconsultancy.com

WEB:
www.jsp-teleconsultancy.com